CLAIMS

1. A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

(a) forming over a semiconductor substrate:

a plurality of first structures projecting upward, each first structure comprising floating gates for a plurality of nonvolatile memory cells associated with the first structure, each first structure comprising a first sidewall which is a dielectric sidewall;

one or more pedestals projecting upward, each pedestal being positioned between the adjacent first sidewalls of two adjacent first structures;

(b) forming a first layer and processing the first layer to provide a plurality of conductive lines, each conductive line overlaying the first sidewall of at least one first structure and providing conductive gates to the memory cells associated with the first structure, wherein each conductive line has a first portion that stretches between the associated first sidewall and an adjacent pedestal and reaches the pedestal, and each conductive line has a second portion that is not located between the first sidewall and a pedestal, the second portion being a sidewall spacer;

wherein the processing of the first layer comprises a first etch of the first layer to form the sidewall spacers for the second portions, the second portions not being protected by a mask during the first etch;

wherein at least one pedestal physically contacts two of the conductive lines having their first portions stretching between the respective two first sidewalls and the pedestal, the two conductive lines being insulated from each other.

2. The method of Claim 1 wherein the first layer as initially formed comprises a portion P1 going around at least said one pedestal, the portion P1 extending between future positions of the two conductive lines which are to physically contact the pedestal; and

said processing of the first layer further comprises removing the portion P1 to insulate the two conductive lines from each other.

3. The method of Claim 2 wherein the removing of the portion P1 includes a second etch of the first layer.

4. The method of Claim 3 wherein the second etch is performed after the first etch.

5. The method of Claim 3 wherein the second etch is a masked etch, with a portion of the first layer subjected to the second etch being defined by a photolithographic mask, wherein the same mask also defines a gate of a peripheral transistor of the integrated circuit.

6. The method of Claim 5 wherein the gate of the peripheral transistor is formed from a layer different from the first layer.

7. The method of Claim 5 wherein each first structure comprises a second sidewall;

wherein the first layer as initially formed comprises portions over the second sidewalls of the first structures; and

said processing of the first layer comprises a third etch which comprises etching the first layer over the second sidewalls but not over the first sidewalls, wherein the area at the location of the first layer portion P1 is exposed to the third etch to enable the third etch to remove the first layer in the exposed area if the first layer remains in the exposed area.

8. The method of Claim 7 wherein the third etch is an isotropic etch.

9. The method of Claim 8 wherein the second etch is an anisotropic etch.

10. The method of Claim 7 wherein the third etch is performed after the second etch.

11. The method of Claim 7 wherein each first structure comprises at least one end between the first and second sidewalls of the first structure, and the first layer as initially formed goes around said ends;

wherein the second etch comprises etching the first layer adjacent to said ends of the first structures, the second etch being an anisotropic etch.

12. The method of Claim 2 wherein each first structure comprises second sidewall;

wherein the first layer as initially formed comprises portions over the second sidewalls of the first structures; and

said processing of the first layer comprises etching the first layer over the second sidewalls but not over the first sidewalls and simultaneously etching the first layer portion P1.

13. The method of Claim 1 wherein each pedestal comprises at least one conductive feature which is a dummy element and not a circuit element of the integrated circuit.

14. The method of Claim 1 wherein the pedestals have no electrical functionality.

15. The method of Claim 1 further comprising depositing a dielectric layer over the conductive lines and forming one or more openings in the dielectric layer to expose the first portions of the conductive lines.

16. The method of Claim 15 further comprising depositing conductive material in the openings to make electrical contact to the conductive lines.

17. The method of Claim 1 wherein each conductive line is a wordline extending along a row of the memory cells.

18. The method of Claim 1 wherein each first structure comprises a conductive control gate line that provides control gates to the associated memory cells.

19. The method of Claim 1 wherein the minimum thickness of the first portions is greater than the minimum thickness of the second portions.

20. The method of Claim 1 wherein the second portions are narrower than the first portions.

21. The method of Claim 1 wherein the first portions are not protected by a mask during the first etch.

22. A method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

(a) forming over a semiconductor substrate:

a plurality of first structures projecting upward, each first structure comprising floating gates for a plurality of nonvolatile memory cells associated with the first structure, each first structure comprising a first sidewall which is a dielectric sidewall;

one or more pedestals projecting upward, each pedestal being positioned between the adjacent first sidewalls of two adjacent first structures;

(b) forming a first layer and processing the first layer to provide a plurality of conductive lines, each conductive line overlaying the first sidewall of at least one first structure and providing conductive gates to the memory cells associated with the first structure, wherein each conductive line has a first portion that stretches between the associated first sidewall and an adjacent pedestal and reaches the pedestal, and each conductive line has a second portion that is not located between the first sidewall and a pedestal, the second portion being a sidewall spacer;

wherein the processing of the first layer comprises a first etch of the first layer to form the sidewall spacers for the second portions, the second portions not being protected by a mask during the first etch;

wherein the first layer as initially formed comprises a portion P1 going around at least said one pedestal, said portion P1 extending between future positions of the two conductive lines which are to physically contact the pedestal; and

said processing of the first layer further comprises removing said portion P1 to insulate the two conductive lines from each other.

23. The method of Claim 22 wherein the removing of the portion P1 includes a second etch of the first layer.

24. The method of Claim 23 wherein the second etch is performed after the first etch.

25. The method of Claim 23 wherein the second etch is a masked etch, with a portion of the first layer subjected to the second etch being defined by a photolithographic mask, wherein the same mask also defines a gate of a peripheral transistor of the integrated circuit.

26. The method of Claim 25 wherein the gate of the peripheral transistor is formed from a layer different from the first layer.

27. The method of Claim 25 wherein each first structure comprises a second sidewall;

wherein the first layer as initially formed comprises portions over the second sidewalls of the first structures; and

said processing of the first layer comprises a third etch which comprises etching the first layer over the second sidewalls but not over the first sidewalls, wherein the areas at the location of the portion P1 is exposed to the third etch to enable the third etch to remove the first layer in the exposed area if the first layer remains in the exposed area.

28. The method of Claim 27 wherein the third etch is an isotropic etch.

29. The method of Claim 28 wherein the second etch is an anisotropic etch.

30. The method of Claim 27 wherein the third etch is performed after the second etch.

31. The method of Claim 27 wherein each first structure comprises at least one end between the first and second sidewalls, and the first layer as initially formed goes around said ends;

wherein the second etch comprises etching the first layer adjacent to said ends of the first structures, the second etch being an anisotropic etch.

32. The method of Claim 22 wherein each first structure comprises a second sidewall;

wherein the first layer as initially formed comprises portions over the second sidewalls of the first structures; and

said processing of the first layer comprises etching the first layer over the second sidewalls but not over the first sidewalls and simultaneously etching the first layer portion P1.

33. The method of Claim 22 wherein each pedestal comprises at least one conductive feature which is a dummy element and not a circuit element of the integrated circuit.

34. The method of Claim 22 wherein the pedestals have no electrical functionality.

35. The method of Claim 22 further comprising depositing a dielectric layer over the conductive lines and forming one or more openings in the dielectric layer to expose the first portions of the conductive lines.

36. The method of Claim 35 further comprising depositing conductive material in the openings to make electrical contact to the conductive lines.

37. The method of Claim 22 wherein each conductive line is a wordline extending along a row of the memory cells.

38. The method of Claim 22 wherein each first structure comprises a conductive control gate line that provides control gates to the associated memory cells.

39. The method of Claim 22 wherein the minimum thickness of the first portions is greater than the minimum thickness of the second portions.

40. The method of Claim 22 wherein the second portions are narrower than the first portions.

41. The method of Claim 22 wherein the first portions are not protected by a mask during the first etch.

42. An integrated circuit comprising:

a semiconductor substrate;

one or more first structures over the semiconductor substrate, the first structures projecting upward, each first structure comprising floating gates for a plurality of nonvolatile memory cells associated with the first structure, each first structure comprising a dielectric sidewall;

one or more pedestals projecting upward over the semiconductor substrate, each pedestal being adjacent to the dielectric sidewall of at least one first structure;

one or more conductive lines, each conductive line overlaying the dielectric sidewall of at least one first structure and providing conductive gates to the memory cells associated with the first structure, wherein the conductive line has a first portion that stretches between the dielectric sidewall and an adjacent pedestal and reaches the pedestal, and the conductive line has a second portion that is not located between the sidewall and a pedestal;

wherein at least one pedestal physically contacts two of the conductive lines having their first portions stretching between the respective two dielectric sidewalls and the pedestal, the two conductive lines being insulated from each other.

43. The integrated circuit of Claim 42 wherein each pedestal comprises at least one conductive feature which is a dummy element and not a circuit element of the integrated circuit.

44. The integrated circuit of Claim 42 wherein the pedestals have no electrical functionality.

45. The integrated circuit of Claim 42 further comprising a dielectric layer over the conductive lines, and one or more openings in the dielectric layer that expose the first portions of the conductive lines.

46. The integrated circuit of Claim 45 further comprising conductive material in the openings to make electrical contact to the conductive lines.

47. The integrated circuit of Claim 42 wherein each conductive line is a wordline extending along a row of the memory cells.

48. The integrated circuit of Claim 42 wherein each first structure comprises a conductive control gate line that provides control gates to the associated memory cells.

49. The integrated circuit of Claim 42 wherein the minimum thickness of the first portions is greater than the minimum thickness of the second portions.

50. The integrated circuit of Claim 42 wherein the second portions are narrower than the first portions.